We Claim:

1. A method for encoding a plurality of data bits for use in communications device, the method comprising:

a) receiving a set of data bits for encoding;

b) encoding in parallel a subset of said set of data bits using at least one other subset of data bits to produce at least one first set of output bits;

c) encoding in parallel said subset of said set of data bits using at least one previous subset of data bits to produce at least one second set of output bits, the or each of said previous subset being a subset of a previous set of data bits.

2. A method according to claim 1 wherein said encoding is convolutional encoding.

3. A method according to claim 1 wherein said set of data bits is divided into two subsets.

4. A method according to claim 3 wherein said subset of said set of data bits is encoded in step b) using the other subset of said set of data bits.

5. A method according to claim 4 wherein said at least one previous subset comprises a single subset of a previous set of data bits, said single subset being a subset which was not encoded for said previous set of data bits.

6. A method for encoding a set of data bits for use in a communications system, the method comprising the steps of:

a) receiving first and second subsets of said set of data bits;

b) convolutionally encoding said first subset using said second subset to produce a first set of output bits;

c) convolutionally encoding said first subset using a previous subset of an immediately

preceding set of data bits to produce a second set of output bits; and

d) replacing said previous subset with said second subset of said set of data bits for use with a next set of data bits,

wherein said encoding in steps b) and c) are executed in a bitwise parallel manner.

7. A method according to claim 6 wherein said steps b) and c) are executed simultaneously.

8. A method according to claim 6 wherein a number of useful bits from said second set of output bits is determined by a predetermined convolutional rate.

9. A device for encoding a set of data bits for use in a communications system, the device comprising:

- first receiving means for receiving and storing a first subset of said set of data bits;
- second receiving means for receiving and storing a second subset of said set of data bits;
- storage means for storing a subset of an immediately preceding set of data bits;
- first encoding means for convolutionally encoding a subset of data bits, said first encoding means receiving inputs from said first receiving means and from said second receiving means to produce a first set of output bits;
- second encoding means for convolutionally encoding a subset of data bits, said second encoding means receiving inputs from said first receiving means and from said storage means to produce a second set of output bits;
- switching means for storing contents of said second receiving means in said storage means,

wherein said storage means and said switching means is activated after said first and second sets of output bits have been produced.

10. A device according to claim 9 wherein said first encoding means and said second encoding means both convolutionally encode in a parallel bitwise manner.

11. A device according to claim 9 wherein said first encoding means and said second encoding means operate simultaneously.

12. A device according to claim 9 wherein said first encoding means comprises an encoding module comprising a plurality of single-bit submodules, each of said single bit submodules receiving a single bit of said first subset and said second subset and producing two output bits produced by convolutionally encoding said single bit using said second subset.

13. A device according to claim 9 wherein said second encoding means comprises an encoding module comprising a plurality of single-bit submodules, each of said single bit submodules receiving a single bit of said first subset and said subset of said immediately preceding set of data bits and producing two output bits produced by convolutionally encoding said single bit using said subset of said immediately preceding set of data bits.

14. A device according to claim 9 wherein each of said single bit submodules implements an XOR operation between said single bit and predetermined bits of said second subset.

15. A device according to claim 13 wherein each of said single bit submodules implements an XOR operation between said single and specific predetermined bits of said subset immediately preceding set of data bits.

16. A system for encoding a current set of data bits for use in a communications device, the device comprising:

- at least two encoding stages for encoding a subset of said current set of data bits, each of said at least two stages comprising:

- first receiving means for receiving and storing a first subset of said current set of data bits;

- storage means for storing a subset of data bits, said subset of data bits being chosen from a group comprising:

- a second subset of said current set of data bits; and

- a subset of a previously received set of data bits,

- encoding means for encoding contents of said first receiving means using contents of said storage means to produce a set of output bits,

wherein at least one encoding stage receives a subset of dat bits form another encoding stage for storage in said storage means and for encoding a subset of said current set of data bits.

17. A system according to claim 16 wherein each encoding means encodes in a parallel bitwise manner.

18. A system according to claim 16 wherein each of said encoding stages operates simultaneously with other encoding stages.

19. A system according to claim 16 wherein said encoding means comprises an encoding module comprising:

a plurality of single bit submodules, each of said single bit submodules receiving said subset of data bits and a single bit of said first subset, each of said single bit submodules producing two output bits produced by convolutionally encoding said single bit using said subset of data bits.

20. A system according to claim 19 wherein each single bit submodule comprises a combinational logic circuit implementing an XOR operation between said single bit and predetermined bits of said subset of data bits.